DTEK1056 Energy Efficient Embedded Systems **FINAL EXAM 26.04.2019**

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This final exam consists of 5 questions (each giving max 6 points) and one extra bonus question (giving 3 extra points), total maximum 30 points (+3). You have 3 hours exam time. Please provide short and accurate answers for each question. No course material is allowed in the exam. Good luck!

1. (a) Explain power consumption sources in CMOS inverter when inverter is changing its logic state at the output. What effects contribute to the power consumption at the input and at the output of the inverter.

(b) Explain how active and standby power consumption contributions have changed during technology scaling from yesterdays 180 nm technology to today's 22 nm CMOS technology. What technology innovations have been used to reduce the power consumption in CMOS logic when we move to today´s 16 nm CMOS production technologies.

2. Explain what power optimization techniques for energy efficiency have been used at logic block level such as multipliers and adders and how the different techniques are scaling in effectiveness when the technology is scaling from 90 nm towards 16 nm.

3. Explain the key techniques for power reduction techniques at chip level at standby (when the chip is not doing any processing) for nanoscale CMOS technology.

4. Explain dynamic voltage and frequency scaling technique for power reduction. What are the key design challenges for power and clock distribution networks in implementing DVFS technique?

5. You are the design team leader in a Wearable Electronics (like smart watches, electronics accessories/jewelry, biosensor) start-up company for a new very small intelligent sensor device for personal monitoring with respect to location, your activity, and various bio-signals. The device is communicating with RF to cloud based serviced, it is doing processing of data from sensors , and finally its is controlling the sensors for measurements. The device need to be extremely low power and have very long battery life time or no battery at all, due to fact is preferably embedded to your clothes or jewelry or watch. As the team leader you are requested to give a short presentation on system solutions and design ideas to a group of investors and to the company top management. Explain shortly what you are going to present as your approach for implementation and design of such device in an allocated 10 minute time slot for your presentation in the meeting between risk capital investors and top management of your company.

6. Extra bonus question. What was the most difficult part to learn from the course? How you would the course to be improved for the following year? What material or content you would like to see added to the course? What you gained from the course?